REMARKS

In the Office Action, the Examiner rejected the claims citing United States Patent Nos. 4,972,144 (Lyon et al.) and 5,289,116 (Kurita et al.).

Claim 1 has been amended and specifically claims a system for testing a plurality of test structures. The system includes a logic circuit which is connectable to a plurality of rows of test structures, and which is configured to receive a triggering signal. Each time the triggering signal changes, the logic circuit sequentially turns on a different single row of test structures such that only a single row is active at any given time during the testing and the remaining rows are inactive. As such, the system is configured to sequentially test the rows of test structures, from a first row to a last row, a single row at a time each time the triggering signal changes. Claim 9 is similar but is directed to a method.

Neither one of the references cited by the Examiner disclose or suggest what is being claimed. For example, the Lyon reference discloses that, during a "Stuck High" Test Mode, a logic "0" is provided on a test line (TL) and only one address line (i.e., the first address line) is set to a low level while the other address lines are set to a high level. Then, the next address line (i.e., the second address line) is set to a low level while the other address lines are set to a high level, and so on (see col. 5, lines 23-36 of the Lyon reference). Contrary to what is being claimed in claim 1 and 9 of the present application, the Lyon reference does not disclose that only a single row is active at any given time during the testing and the remaining rows are inactive. In fact, the Lyon reference teaches the opposite - only a single address line is set to a low level while all the other address lines are set to a high level. Additionally, contrary to what is being claimed in

claim 1 and 9 of the present application, the Lyon reference does not disclose that each time the triggering signal changes, a logic circuit sequentially turns on a different single row of test structures. Instead, in the Lyon reference, the test line (TL) "is a signal line to provide signals which switch the decoder 10 to a normal operation mode or a test mode" (See col 3, lines 27-29 of the Lyon reference). The Lyon reference does not disclose, for example, that each time the signal on the test line changes, a different single row of test structures is turned on.

Applicant respectfully submits that neither one of the references cited by the Examiner, either alone or in combination, can be said to provide what is being specifically claimed in claims 1 and 9. Therefore, Applicant respectfully asserts that claims 1 and 9, and those claims which depend therefrom, are allowable.

The present application has been amended in response to the Examiner's Office Action to place the application in condition for allowance. Applicant, by the amendments and remarks presented above, has made a concerted effort to present claims which clearly define over the prior art of record, and thus to place this case in condition for allowance.

Should the present claims not be deemed adequate to effectively define the patentable subject matter, the Examiner is respectfully urged to call the undersigned attorney of record to discuss the claims in an effort to reach an agreement toward allowance of the present application.

Respectfully submitted,

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By: _____

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